REMARKS

Claims 2-4, 6-10, 12, and 14-18 are pending in this application, with claims 2, 6, 12, and 14 being independent. Claims 1, 5, 11, and 13 have been cancelled. Claims 2, 3, 6, 12, 14, and 15 have been amended. No new matter has been introduced.

For the reasons set forth below, Applicants respectfully submit that all pending claims as currently amended are patentable over the cited prior art.

Allowable Subject Matter

As a preliminary matter, Applicants thank the Examiner for indicating that claims 3, 4, 7-10, 12, 14, and 16-18 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. In reliance on the Examiner's assertion, Applicants have amended claims 12 and 14 to place them in independent form. Therefore, Applicants respectfully request that claims 12 and 14 be allowed at this time. Furthermore, Applicants respectfully request allowance of claims 16-18 because claims 16-18 variously depend from indicated allowable claim 14.

Claims 3, 4, and 7-10 are not rewritten in independent form. However, Applicants respectfully request the withdrawal of the rejection of claims 3, 4, and 7-10 because they depend either from claim 2 or 6, both of which are allowable over the cited prior art for at least the reasons described in more detail below.

Rejections Under 35 U.S.C. § 102

Claims 1, 2, 5, and 6 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Number 6,370,162 ("Takahashi"). With respect to canceled claims 1 and 5, this

rejection is rendered moot. With respect to claims 2 and 6, Applicants respectfully traverse their rejections for at least the following reasons.

As amended, claim 2 recites a data transmitting/receiving device, comprising a serial-parallel conversion circuit for converting received first serial data to first parallel data; a data selection circuit for selecting any one of the first parallel data and externally-supplied second parallel data and outputting the selected data; and a parallel-serial conversion circuit for converting the first or second parallel data output from the data selection circuit to second serial data which is to be transmitted, wherein the parallel-serial conversion circuit receives a common clock signal with the serial-parallel conversion circuit and operates in synchronization with the common clock signal when the data selection circuit selects the first parallel data.

Applicants respectfully request reconsideration and withdrawal of the rejection of claim 2 and its dependent claims because at a minimum Takahashi fails to describe or suggest a data transmitting/receiving device including, among other features, a parallel-serial conversion circuit receives a common clock signal with a serial-parallel conversion circuit and operates in synchronization with the common clock signal when a data selection circuit selects first parallel data, as recited in claim 2 (emphasis added).

Takahashi, in FIG. 1, discloses a frame aligner having a serial/parallel converter (1), a first buffer (2-1), a second buffer (2-2), a selector (3), and a parallel/serial converter (4). Takahashi at Abstract. The serial/parallel converter (1) converts an input serial data signal into a first parallel data signal using the input clock signal CK_{in}. Takahashi at col. 2, lines 46-52. The first buffer (2-1) receives the first parallel data signal and generates a first parallel data signal (S_2), and the second buffer (2-2) receives the first parallel data signal and generates a second parallel data signal (S_3). Takahashi at Abstract. The selector (3) selects between one of the first

and second parallel data signals (S_2, S_3) and generates a third parallel data signal (S_3). Takahashi at Abstract. The parallel-serial converter (4) performs parallel serial conversion upon the third parallel data signal (S_3) and generates an output serial data signal using clock signal CK_{out}. Takahashi at col. 2, lines 57-61.

Although Takahashi appears to describe a serial/parallel converter (1) and a parallel/serial converter (4), it does not appear to describe or suggest a parallel-serial conversion circuit that receives a common clock signal with a serial-parallel conversion circuit, as recited in claim 2 (emphasis added). Indeed and to the contrary, Takahashi describes that the serial/parallel converter (1) and the parallel/serial converter (4) each receive a different clock signal. Takahashi at col. 3, lines 60-62 (stating that "a difference in phase between the output clock signal CK_{out} and the input clock signal CK_{in} varies").

Accordingly, Takahashi cannot describe or otherwise suggest a data transmitting/receiving device including, among other features, a parallel-serial conversion circuit receives a common clock signal with a serial-parallel conversion circuit and operates in synchronization with the common clock signal when a data selection circuit selects first parallel data, as recited in claim 2 (emphasis added).

In one aspect, the present invention enables measurement of jitter tolerance because the parallel-serial conversion circuit receives a common clock signal with the serial-parallel conversion circuit and operates in synchronization with the common clock signal when the data selection circuit selects the first parallel data. For at least the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 2, along with its dependent claims.

Claim 6 includes features similar to the above-recited features of claim 2. Therefore, for at least the reasons presented above with respect to claim 2, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 6, along with its dependent claims.

Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Because claims 2, 6, and 14 are allowable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also allowable. In addition, it is respectfully submitted that the dependent claims are allowable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Therefore, it is respectfully requested that the rejection under § 102 be withdrawn.

Conclusion

Accordingly, it is believed that all pending claims are now in condition for allowance. Applicants therefore respectfully request an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicants' representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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